#10/Appeal Brief 3/9/04 K Pham

Atty Docket No. 04860.P2438

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Biyabani, Sara R.
Serial No. 09/589,621
Filed: June 7, 2000
For: Decoupling a Color Buffer from Main Memory

Examiner: Caschera, A.
Art Unit: 2697

Mail Stop Appeal Brief- Patents
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P.O. Box 1450
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APPELLANT'S BRIEF UNDER 37 C.F.R. 1.192

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner of Group 2697, dated August 27, 2003, which finally rejected the claims in the above-identified application. This Appeal Brief is hereby submitted in triplicate pursuant to 37 C.F.R. § 1.192(a).

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the full interest in the invention, Apple Computer, Inc., 1 Infinite Loop, Cupertino, California.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

III. STATUS OF THE CLAIMS

Claims 1-26 are pending in the application and were finally rejected in an Office Action mailed August 27, 2003. Claims 1-26 are the subject of this appeal. A copy of Claims 1-26 as they stand on appeal are set forth in Appendix A.

IV. STATUS OF AMENDMENTS

Appellant filed the application with claims 1-21 on June 7, 2000. A first Office Action mailed on November 5, 2002 rejected claims 1-21. In a response mailed February 5, 2003, Appellant amended claims 1, 2, 10, 11, 15 16 and 21, and added new claims 22-26. A second, non-final Office Action mailed March 28, 2003 rejected claims 1-26. In a response mailed June 30, 2003, Appellant amended claims 1, 10, 15 and 22. A final Office Action mailed August 27, 2003 finally rejected claims 1-26.

V. SUMMARY OF INVENTION

Appellant's invention as claimed in claims 1-26 is a sole memory controller used to manage use of a main memory between a graphics subsystem and a processing unit in a unified memory architecture computer system [Specification: page 10, line 16 through page 11, line 4]. In one embodiment, the memory controller decouples memory used for a color buffer from the main memory and logically divides the color buffer into address spaces for a frame-preparation memory and for a refresh memory. The memory controller logically connects the frame-preparation memory to the graphics subsystem, which writes color data into the frame-preparation memory at a frame rate, and logically connects the refresh memory to a display device, which reads the color data from the refresh memory at a refresh rate. [Specification: page 11, line 5 though page 12, line 9; Figure 2] In an alternate embodiment, the memory controller further logically divides the color buffer in to an address space for a transfer memory. The memory controller copies color data that is ready for display from the transfer memory to the refresh memory. [Specification: page 12, line 20 through page 13, line 17; Figure 3]

VI. ISSUES

I. Whether Claims 1-3, 5, 10-12, 15-16, 18, and 22-24 are patentable under 35 U.S.C. § 103(a) over the combination of Stortz (U.S. Patent 5,900,885), Asaro et al. (U.S. Patent 6,100,906), Chan et al. (U.S. Patent 6,184,908 B1) and Norsworth et al. (U.S. Patent 5,241,641).

II. Whether Claims 4, 13, 17 and 25 are patentable under 35 U.S.C. § 103(a) over the combination of Stortz, Asaro, Chan, Norsworth and Swan (U.S. Patent 6,184,908 B1).

III. Whether Claims 6-9, 14, 19-21 and 26 are patentable under 35 U.S.C. § 103(a) over the combination of Stortz, Asaro, Chan, Norsworth and Naughton (U.S. Patent 5,519,825).

VII. GROUPING OF CLAIMS

I. Group I consists of Claims 1-3, 5, 10-12, 15-16, 18, and 22-24 that stand rejected on the grounds presented as Issue I. Claims 1-3, 5, 10-12, 15-16, 18, and 22-24 stand or fall together. Claim 1 is the representative claim for Group I.

II. Group II consists of Claims 4, 13, 17 and 25 that stand rejected on the grounds presented as Issue II. Claims 4, 13, 17 and 25 stand or fall together. Claim 4 is the representative claim for Group II.

III. Group III consists of Claims 6-9, 14, 19-21 and 26 that stand rejected on the grounds presented as Issue II. Claims 6-9, 14, 19-21 and 26 stand or fall together. Claim 6 is the representative claim for Group III.

VIII. ARGUMENTS

I. Claims 1-3, 5, 10-12, 15-16, 18, and 22-24 are Patentable under 35 U.S.C. § 103(a) over the combination of Stortz, Asaro, Chan and Norsworth.

Stortz discloses a video controller that controls video memory on a graphics card and can use a portion of system memory that has been de-allocated from the system memory controller as an incremental video buffer. The deallocation is necessary to

prevent contention between the CPU and the graphics card for the memory and is performed by either the BIOS or through modification of the system controller. The system controller manages the use of the remainder of the system memory by the CPU. Stortz does not teach or suggest that the portion of system memory can be re-allocated to the system memory controller. Thus, Stortz teaches using two different components to control memory in the system, a system memory controller to control the system memory used by the CPU and a video controller to control the video memory and the incremental video buffer.

Asaro discloses a video processing module that manages two buffers in a dedicated video memory. Separate system memory is controlled by the CPU. Thus, like Stortz, Asaro teaches using two different components to control memory in the system, the video controller to control the dedicated video memory and the CPU to control the system memory.

Chan discloses a graphics command processor having dedicated memory that is used as a partitioned buffer and a command buffer. An application program executing on the CPU of the system stores commands and raw vertex data into a system memory for processing by the graphics command processor. A fetcher component of the graphics command processor retrieves the commands and raw vertex data from the system memory and stores them into two different partitions in the partitioned buffer for subsequent processing by a vertex processor and a command parser. After processing, the resulting commands and vertex data are stored in the command buffer for output to a graphics engine and eventual display. Thus, Chan, teaches using two different components, the CPU and the fetcher, to control the portion of system memory that holds the input to the graphics command processor. Furthermore, Chan also teaches that the partitioned and command buffers are controlled by the graphics command processor, not the CPU.

Norsworthy discloses a unified address space that allows different types of video memory, ex., DRAM and VRAM, to be addressed as a single memory. The unified address space is set up and controlled by an image memory controller. The CPU sends data to the image memory controller but the CPU cannot directly access the video

memory through the image memory controller. Thus, Norsworthy is directed only to the management of video memory, not a main memory.

In claim 1, Appellant claims a sole memory controller for a unified memory architecture that is operable to

1) manage use of main memory between a graphics subsystem and a processing unit;

2) partition an address space for a color buffer in main memory into two logical buffers;

3) designate one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory;

4) connect the frame-preparation memory to the graphics subsystem to write color data into the frame-preparation memory at a frame rate; and

5) connect the refresh memory to a display device to read color data from the refresh memory at a rate that supports a refresh rate of the display device.

The Examiner asserts Stortz discloses a system memory controller that manages uses of main memory between a graphics card (subsystem) and a processing unit to find equivalence with Appellant's claimed sole memory controller that manages use of a main memory between a graphics subsystem and a processing unit. Appellant respectfully submits that this is an incorrect interpretation of Stortz. Stortz actually teaches that the video controller de-allocates the portion of main memory from processing unit and subsequently controls its use. The system controller has no control over the incremental video buffer once it has been de-allocated by the video controller and therefore cannot control its use by either the CPU or the graphics card.

The Examiner also asserts Stortz teaches that the system memory controller assigns the incremental video buffer in main memory and the decoupled video buffer in video memory to find equivalence with Appellant's claimed sole memory controller that designates memory as a frame-preparation memory and a refresh memory. Appellant respectfully submits that this is also an incorrect interpretation of Stortz. In fact, Stortz teaches that the video controller does the assignment, not the system memory controller.

The Examiner asserts that Asaro teaches writing into one of two buffers at a frame rate and that the buffers are flipped at a refresh rate for reading to find equivalent with

Appellant's claimed memory controller operation that writes color data into the frame-preparation memory at a frame rate and reads the color data from the refresh memory at a rate that supports a refresh rate of the display device Appellant respectfully submits that this is a misinterpretation Asaro. Asaro actually teaches that data is written into a buffer "at any rate" selected by the CPU, including a rate that is independent of the graphics co-processor and independent of the refresh rate. A frame rate is not taught nor suggested. Furthermore, Asaro does not teach or suggest that the data is read from a buffer at the refresh rate of a display. Instead Asaro teaches that the buffers are flipped at most once per refresh cycle, which Asaro states is the inverse of the refresh rate. In addition, the buffers are only flipped if the current data is ready for display. If not, the flip is postponed for another refresh cycle and nothing is read from the display buffer.

The Examiner asserts that Chan's partitioned buffer holding raw vertex data is equivalent to Appellant's claimed color buffer. However, Chan's partitioned buffer is only divided into two parts, one of which holds the commands. In contrast, Appellant claims the sole memory controller further partitions the color buffer itself into two logical buffers. Chan discloses that the sizes of the first and second logical buffers may be adjusted, but does not teach or suggest further dividing the buffer or memory holding the raw vertex data into two logical buffers.

The Examiner has cited Norsworthy as evidence of a unified memory architecture to support the Examiner's argument that it would be obvious to combine the teachings of Stortz, Asaro and Chan into a single memory controller as claimed by Appellant. Appellant respectfully submits that this is an misinterpretation of Norsworthy. Norsworthy actually discloses a unified *address space* so that different types of video memory can be access through a common address space. Unified memory architecture is a term of art commonly accepted as referring to an architecture in which main memory is shared among the components of the system. A unified address space for video memory is not equivalent to a unified memory architecture having a shared main memory. Moreover, Norsworthy discloses the image memory controller only controls the video memory, and does not teach or suggest that the image memory controller controls the main memory in the system as required within a unified memory architecture.

Therefore, the combination of Stortz, Asaro, Chan and Norsworth does not teach each and every limitation of Appellant's invention as claimed in claim 1 and accordingly Appellant's claims 1-3, 5, 10-12, 15-16, 18, and 22-24 are patentable under 35 U.S.C. § 103 over the combination.

II. Claims 4, 13, 17 and 25 are Patentable under 35 U.S.C. § 103(a) over the combination of Stortz, Asaro, Chan, Norsworth and Swan.

Swan discloses a video process that adjusts video rates by adding or deleting frames in video output from a graphics processor. The frame buffer may be divided into two sections. While data is being written into one section, previously written data is being read from the other. The sections are flipped when the writing of the data is complete. As known in the art, data should be written into the frame buffer at the display refresh rate to produce the best output. However, if the writing is slower or faster, Swan adjusts the output rate by adding or deleting frames at locations that are determined to have the minimal adverse effect on the display.

Claim 4 depends from claim 3, which depends from claim 1. Claim 4 adds the limitation that the memory controller copies the color data from the frame-preparation memory to the refresh memory at pre-determined intervals.

The Examiner is equating the two sections of Swan's frame buffer to Appellant's claimed frame-preparation memory and refresh memory. However, Swan does not disclose that frame data is copied between the two sections of the frame buffer but instead that the sections are flipped.

Therefore, the combination of Stortz, Asaro, Chan, Norsworth and Swan does not teach each and every limitation of Appellant's invention as claimed in claim 4 and accordingly Appellant's claims 4, 13, 17 and 25 are patentable under 35 U.S.C. § 103 over the combination.

III. Claims 6-9, 14, 19-21 and 26 are Patentable under 35 U.S.C. § 103(a) over the combination of Stortz, Asaro, Chan, Norsworth and Naughton.

Naughton discloses a video cache buffer that stores a subset of data used to create a video frame for display. The central processing unit (CPU) partitions a separate video

memory (VRAM) into three buffers. Two of the buffers are used as frame buffers and the third buffer is dedicated to caching video data from the CPU before it is written into the frame buffers. While data is being written from the cache buffer into one of the frame buffers, previously written data is being read out of the other. When the writing is complete, the buffers are flipped.

Claim 6 depends from claim 1 and adds the further limitations that the memory controller 1) partitions the address space for the color buffer into a third logical buffer, 2) designates the third logical buffer as a transfer memory, and 3) copies the color data from the transfer memory to the refresh memory. Thus, the transfer memory is logically coupled to the refresh memory, which is further coupled to the display as claimed in claim 1.

The Examiner is equating Naughton's cache buffer to Appellant's claimed transfer buffer and Naughton's two frame buffers to Appellant's claimed frame-preparation memory and refresh memory. However, the data in Naughton's cache buffer is not written to the frame buffer that is currently connected to the display, but instead is written into the frame buffer that is not connected to the display.

Therefore, the combination of Stortz, Asaro, Chan, Norsworth and Naughton does not teach each and every limitation of Appellant's invention as claimed in claim 6 and accordingly Appellant's claims 6-9, 14, 19-21 and 26 are patentable under 35 U.S.C. § 103 over the combination

IX. CONCLUSION

Because the combinations cited by the Examiner's in rejecting Appellant's claims under 35 U.S.C. § 103(a) does not teach each and every limitation of the claims, Appellant respectfully requests the Board reverse the rejections of claims 1-26 under 35 U.S.C. § 103(a) and direct the Examiner to enter a Notice of Allowance for claims 1-26.

Fee for Filing a Brief in Support of Appeal

Enclosed is a check in the amount of $ 330.00 to cover the fee for filing a brief in support of an appeal as required under 37 C.F.R. 1.17(c) and 1.192(a).

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Appellant hereby requests such extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR
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Dated: March 1, 2004

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APPENDIX A FOR
APPELLANT'S BRIEF UNDER 37 C.F.R. 1.192

1. (Previously Presented) A unified memory architecture that decouples a color buffer from a main memory in a computer, the architecture comprising:

a sole memory controller connected to the main memory to manage use of the main memory between a graphics subsystem and a processing unit, the memory controller operable for partitioning an address space for the color buffer in main memory into two logical buffers, operable for designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory, operable for connecting the frame-preparation memory to the graphics subsystem and operable for connecting the refresh memory to a display device, wherein color data is written into the frame-preparation memory at a frame rate and read from the refresh memory at a rate that supports a refresh rate of the display device.

2. (Previously Presented) The unified memory architecture of claim 1, wherein the address space for the refresh memory is mapped into a physical memory device for a dedicated memory that is separate from a physical memory device for the main memory.

3. (Previously Presented) The unified memory architecture of claim 1, wherein the memory controller is further operable for copying the color data from the frame-preparation memory to the refresh memory.

4. (Previously Presented) The unified memory architecture of claim 3, wherein the memory controller copies the color data at pre-determined intervals.

5. (Original) The unified memory architecture of claim 3, wherein the memory controller copies the color data when an entire frame of color data is ready for display.

6. (Previously Presented) The unified memory architecture of claim 1, wherein the memory controller is further operable for further partitioning the address space for the color buffer into a third logical buffer, for designating the third logical buffer as a transfer memory, and for copying the color data from the transfer memory to the refresh memory.

7. (Previously Presented) The unified memory architecture of claim 6, wherein the memory controller is further operable for disconnecting the logical buffer currently designated as the frame-preparation memory from the graphics subsystem, and connecting the logical buffer currently designated as the transfer memory to the graphics subsystem to switch the designations of the logical buffers.

8. (Previously Presented) The unified memory architecture of claim 7, wherein the memory controller switches the designations of the logical buffers when an entire frame of color data is ready for display in the logical buffer currently designated as the frame-preparation memory.

9. (Previously Presented) The unified memory architecture of claim 1, wherein the memory controller is operable for connecting the logical buffer currently designated as the frame-preparation memory to the display device and the logical buffer currently designated as the refresh memory to the graphics subsystem to switch the designations of the logical buffers.

10. (Previously Presented) A method of decoupling a color buffer from a main memory by a sole memory controller in a computer having a unified memory architecture, the memory controller managing use of the main memory between a graphics subsystem and a processing unit, the method comprising:

partitioning an address space for the color buffer in the main memory into first and second logical buffers;

designating the first logical buffer as a refresh memory and designating the second logical buffer as a frame-preparation memory;

writing color data into the frame-preparation memory at a frame rate;

copying the color data from the frame-preparation memory to the refresh memory; and

reading the color data from the refresh memory at a rate that supports a refresh rate of a display device.

11. (Previously Presented) The method of claim 10, further comprising:

mapping the address space for the refresh memory onto a physical memory device for a dedicated memory separate from a physical memory device for the main memory.

12. (Previously Presented) The method of claim 10, wherein the color data is copied from the frame-preparation memory to the refresh memory when an entire frame of color data is ready for display.

13. (Previously Presented) The method of claim 10, wherein the color data is copied from the frame-preparation memory to the refresh memory at pre-determined intervals.

14. (Previously Presented) The method of claim 10, further comprising:

further partitioning the address space of the color buffer into a third buffer;

designating the third buffer as a transfer memory;

building a first frame of color data in the frame-preparation memory;

switching the designation of the second buffer with the designation of the third buffer when the first frame of color data is ready for display;

building a second frame of color data in the frame-preparation memory; and

switching the designation of the third buffer with the designation of the second buffer when the second frame of color data is ready for display,

wherein copying the color data from the frame-preparation memory to the refresh memory is accomplished by copying the color data from the buffer currently designated as the transfer memory.

15. (Previously Presented) A computer system having a unified memory architecture, the computer system comprising:

a processing unit;

a main memory connected to the processing unit though a system bus, the main memory being partitioned into an address space for a color buffer;

a sole memory controller connected to the main memory to manage use of the main memory between a graphics subsystem and the processing unit;

a graphics subsystem connected to the main memory through the memory controller to create a frame of color data in the color buffer at a frame rate; and

a display device connected to the main memory through the memory controller, to display a frame of color data from the color buffer at a refresh rate,

wherein the memory controller decouples the color buffer from the main memory by:

partitioning the address space for the color buffer in main memory into two logical buffers;

designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory;

connecting the frame-preparation memory to the graphics subsystem;

connecting the refresh memory to the display device; and

copying the color data from the frame-preparation memory to the refresh memory.

16. (Previously Presented) The computer system of claim 15, further comprising a memory device for a dedicated memory separate from a memory device for the main memory and the memory controller further maps the address space for the refresh memory to the memory device for the dedicated memory.

17. (Previously Presented) The computer system of claim 15, wherein the memory controller copies the color data at pre-determined intervals.

18. (Previously Presented) The computer system of claim 15, wherein the memory controller copies the color data when an entire frame of color data is ready for display.

19. (Previously Presented) The computer system of claim 15, wherein the memory controller further partitions the address space for the color buffer into a third logical buffer, designates the third logical buffer as a transfer memory and copies the color data from the transfer memory to the refresh memory in lieu of copying the color data from the frame-preparation memory.

20. (Previously Presented) The computer system of claim 19, wherein the memory controller further switches the designations of the logical buffers by connecting the logical buffer currently designated as the frame-preparation memory to the display system and by connecting the logical buffer currently designated as the transfer memory to the graphics subsystem.

21. (Previously Presented) The computer system of claim 20, wherein the memory controller switches the designations of the logical buffers when an entire frame of color data is ready for display in the logical buffer currently designated as the frame-preparation memory.

22. (Previously Presented) An apparatus for use in a unified memory architecture comprising:

means for preparing color data for display; and

a sole means for controlling use of a main memory between the means for preparing and a processing unit, for partitioning an address space in the main memory that represents a color buffer into first and second logical buffers, for designating the first logical buffer as a refresh memory and the second logical buffer as a frame-preparation memory, for writing the color data into the frame-preparation memory at a frame rate, for copying the color data from the frame-preparation memory to the refresh memory, and for reading the color data from the refresh memory at a rate that supports a refresh rate of a display device.

23. (Previously Presented) The apparatus of claim 22, wherein the means for controlling further maps the address space for the refresh memory onto a physical memory device for a dedicated memory separate from a physical memory device for the main memory.

24. (Previously Presented) The apparatus of claim 22, wherein the means for controlling copies the color data from the frame-preparation memory to the refresh memory when an entire frame of color data is ready for display.

25. (Previously Presented) The apparatus of claim 22, wherein the means for controlling copies the color data from the frame-preparation memory to the refresh memory at pre-determined intervals.

26. (Previously Presented) The apparatus of claim 22, wherein the means for controlling is further operable for partitioning the address space of the color buffer into a third buffer, designating the third buffer as a transfer memory, building a first frame of color data in the frame-preparation memory, switching the designation of the second buffer with the designation of the third buffer when the first frame of color data is ready for display, building a second frame of color data in the frame-preparation memory, and switching the designation of the third buffer with the designation of the second buffer when the

second frame of color data is ready for display, and wherein the means for controlling copies the color data from the frame-preparation memory to the refresh memory by copying the color data from the buffer currently designated as the transfer memory.